Intro to Quartus II CAD and Verilog HD

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10/11

Post-Lab Analysis

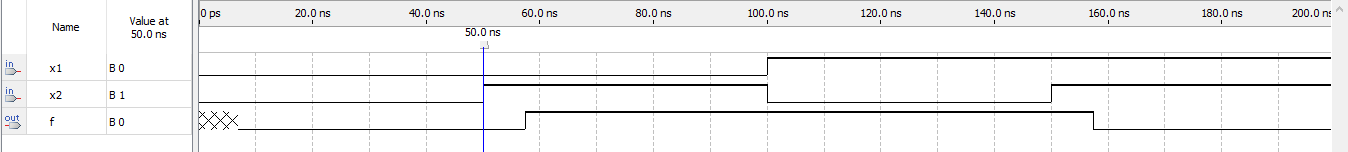
a.

Graphical user interface, text, application

Description automatically generated

Graphical user interface

Description automatically generatedb. functional

timing

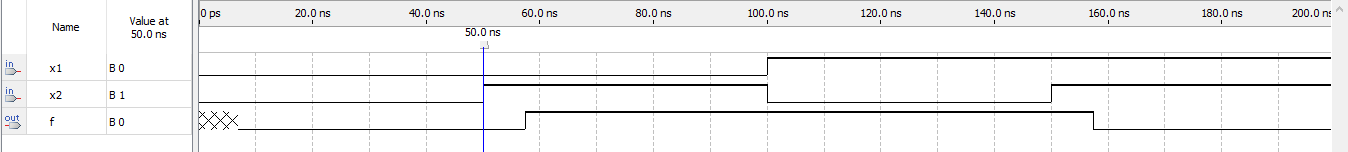
c.

A picture containing diagram

Description automatically generated

Graphical user interface

Description automatically generatedd. functional

timing

2. Simulations through Verilog code and the Schematic diagram both produce the same output diagram. Quartus allows functional and timing simulations on any user created circuit. A functional simulation displays a user input timing diagram with a final output only if, user-circuit sustains no errors. The timing simulation is the same as functional additionally, the output incorporates a time delay alternating the output.

3. <https://electronics.stackexchange.com/questions/135597/what-would-make-me-choose-verilog-or-vhdl-over-schematic-design-on-cplds-or-fpga> User posted by: [wailashi](https://electronics.stackexchange.com/users/4753/wailashi)

He states the schematic function are “buggier” than the benchmark Verilog. Schematic also is transformed into HDL before creating output; moreover, speed is hindered by the conversion. The last reason was the portability of information, schematics only options are recreating the schematic or an external storage device. The author slandered the schematic version, pros for Verilog out way the schematic. More complicated circuits and speed is maximized due to no conversions brings the Verilog version more appealing.